

## Low-Cost 3.3 V Zero Delay Buffer

The MPC962309 is a zero delay buffer designed to distribute high-speed clocks. Available in a 16-pin SOIC or TSSOP package, the device accepts one reference input and drives nine low-skew clocks. The MPC962305 is the 8-pin version of the MPC962309 which drives five outputs with one reference input. The -1H versions of these devices have higher drive than the -1 devices and can operate up to 100/-133 MHz frequencies. These parts have on-chip PLLs which lock to an input clock presented on the REF pin. The PLL feedback is on-chip and is obtained from the CLOCKOUT pad.

### Features

- 1:5 LVCMOS zero-delay buffer (MPC962305)
- 1:9 LVCMOS zero-delay buffer (MPC962309)
- Zero input-output propagation delay
- Multiple low-skew outputs
- 250 ps max output-output skew
- 700 ps max device-device skew
- Supports a clock I/O frequency range of 10 MHz to 133 MHz, compatible with CPU and PCI bus frequencies
- Low jitter, 200 ps max cycle-cycle, and compatible with Pentium® based systems
- Test Mode to bypass PLL (MPC962309 only. See "Select Input Decoding")
- 8-pin SOIC or 8-pin TSSOP package (MPC962305); 16-pin SOIC or 16-pin TSSOP package (MPC962309)
- Single 3.3 V supply
- Ambient temperature range: -40°C to +85°C
- Compatible with the CY2305, CY23S05, CY2309, CY23S09
- Spread spectrum compatible

### Functional Description

The MPC962309 has two banks of four outputs each, which can be controlled by the Select Inputs as shown in [Table 3. Select Input Decoding for MPC962309](#). Bank B can be tri-stated if all of the outputs are not required. Select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The MPC962305 and MPC962309 PLLs enter a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate, the PLL is turned off, and there is less than 25.0  $\mu$ A of current draw for the device. The PLL shuts down in one additional case as shown in [Table 3. Select Input Decoding for MPC962309](#).

Multiple MPC962305 and MPC962309 devices can accept the same input clock and distribute it throughout the system. In this situation, the difference between the output skews of two devices will be less than 700 ps.

All outputs have less than 200 ps of cycle-cycle jitter. The input-to-output propagation delay on both devices is guaranteed to be less than 350 ps and the output-to-output skew is guaranteed to be less than 250 ps.

The MPC962305 and MPC962309 are available in two/three different configurations, as shown on the ordering information page. The MPC962305-1/MPC962309-1 are the base parts. High drive versions of those devices, MPC962305-1H and MPC962309-1H, are available to provide faster rise and fall times of the base device.

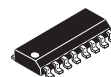
## MPC962305 MPC962309



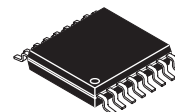
**D SUFFIX**  
8-LEAD SOIC PACKAGE  
CASE 751-06



**DT SUFFIX**  
8-LEAD TSSOP PACKAGE  
CASE 948J-01

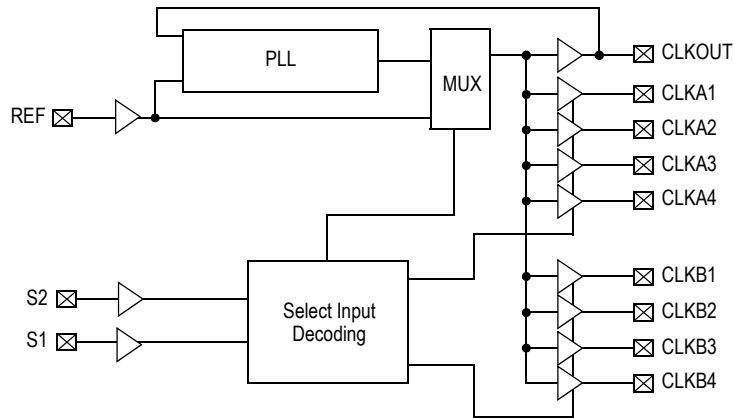


**D SUFFIX**  
16-LEAD SOIC PACKAGE  
CASE 751B-05



**DT SUFFIX**  
16-LEAD TSSOP PACKAGE  
CASE 948F-01

Block Diagram



Pin Configuration

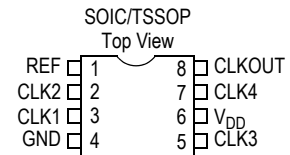
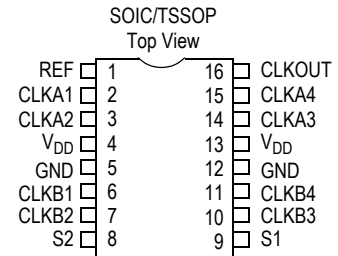


Table 1. Pin Description for MPC962309

| Pin | Signal              | Description                                    |
|-----|---------------------|------------------------------------------------|
| 1   | REF <sup>1</sup>    | Input reference frequency, 5 V-tolerant input  |
| 2   | CLKA1 <sup>2</sup>  | Buffered clock output, Bank A                  |
| 3   | CLKA2 <sup>2</sup>  | Buffered clock output, Bank A                  |
| 4   | V <sub>DD</sub>     | 3.3 V supply                                   |
| 5   | GND                 | Ground                                         |
| 6   | CLKB1 <sup>2</sup>  | Buffered clock output, Bank B                  |
| 7   | CLKB2 <sup>2</sup>  | Buffered clock output, Bank B                  |
| 8   | S2 <sup>3</sup>     | Select input, bit 2                            |
| 9   | S1 <sup>3</sup>     | Select input, bit 1                            |
| 10  | CLKB3 <sup>2</sup>  | Buffered clock output, Bank B                  |
| 11  | CLKB4 <sup>2</sup>  | Buffered clock output, Bank B                  |
| 12  | GND                 | Ground                                         |
| 13  | V <sub>DD</sub>     | 3.3 V supply                                   |
| 14  | CLKA3 <sup>2</sup>  | Buffered clock output, Bank A                  |
| 15  | CLKA4 <sup>2</sup>  | Buffered clock output, Bank A                  |
| 16  | CLKOUT <sup>2</sup> | Buffered output, internal feedback on this pin |

Table 2. Pin Description for MPC962305

| Pin | Signal              | Description                                          |
|-----|---------------------|------------------------------------------------------|
| 1   | REF <sup>1</sup>    | Input reference frequency, 5 V-tolerant input        |
| 2   | CLK2 <sup>2</sup>   | Buffered clock output                                |
| 3   | CLK1 <sup>2</sup>   | Buffered clock output                                |
| 4   | GND                 | Ground                                               |
| 5   | CLK3 <sup>2</sup>   | Buffered clock output                                |
| 6   | V <sub>DD</sub>     | 3.3 V supply                                         |
| 7   | CLK4 <sup>2</sup>   | Buffered clock output                                |
| 8   | CLKOUT <sup>2</sup> | Buffered clock output, internal feedback on this pin |

1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.

## Freescale Semiconductor, Inc.

## MPC962305 MPC962309

Table 3. Select Input Decoding for MPC962309

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | CLKOUT <sup>1</sup> | Output Source | PLL Shutdown |
|----|----|-------------|-------------|---------------------|---------------|--------------|
| 0  | 0  | Three-State | Three-State | Driven              | PLL           | N            |
| 0  | 1  | Driven      | Three-State | Driven              | PLL           | N            |
| 1  | 0  | Driven      | Driven      | Driven              | Reference     | Y            |
| 1  | 1  | Driven      | Driven      | Driven              | PLL           | N            |

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Table 4. Maximum Ratings

| Characteristics                                         | Value                | Unit |
|---------------------------------------------------------|----------------------|------|
| Supply Voltage to Ground Potential                      | –0.5 to +3.9         | V    |
| DC Input Voltage (Except Ref)                           | –0.5 to $V_{DD}+0.5$ | V    |
| DC Input Voltage REF                                    | –0.5 to 5.5          | V    |
| Storage Temperature                                     | –65 to +150          | °C   |
| Junction Temperature                                    | 150                  | °C   |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | >2000                | V    |

Table 5. Operating Conditions for MPC962305-X and MPC962309-X Industrial Temperature Devices

| Parameter | Description                                 | Min | Max | Unit |
|-----------|---------------------------------------------|-----|-----|------|
| $V_{DD}$  | Supply Voltage                              | 3.0 | 3.6 | V    |
| $T_A$     | Operating Temperature (Ambient Temperature) | –40 | 85  | °C   |
| $C_L$     | Load Capacitance, below 100 MHz             |     | 30  | pF   |
| $C_L$     | Load Capacitance, from 100 MHz to 133 MHz   |     | 10  | pF   |
| $C_{IN}$  | Input Capacitance                           |     | 7   | pF   |

Table 6. Electrical Characteristics for MPC962305-X and MPC962309-X Industrial Temperature Devices<sup>1</sup>

| Parameter          | Description                      | Test Conditions                                          | Min | Max   | Unit |
|--------------------|----------------------------------|----------------------------------------------------------|-----|-------|------|
| $V_{IL}$           | Input LOW Voltage <sup>2</sup>   |                                                          |     | 0.8   | V    |
| $V_{IH}$           | Input HIGH Voltage <sup>2</sup>  |                                                          | 2.0 |       | V    |
| $I_{IL}$           | Input LOW Current                | $V_{IN} = 0$ V                                           |     | 50.0  | μA   |
| $I_{IH}$           | Input HIGH Current               | $V_{IN} = V_{DD}$                                        |     | 100.0 | μA   |
| $V_{OL}$           | Output LOW Voltage <sup>3</sup>  | $I_{OL} = 8$ mA (–1)<br>$I_{OH} = 12$ mA (–1H)           |     | 0.4   | V    |
| $V_{OH}$           | Output HIGH Voltage <sup>3</sup> | $I_{OH} = -8$ mA (–1)<br>$I_{OL} = -12$ mA (–1H)         | 2.4 |       | V    |
| $I_{DD}$ (PD mode) | Power Down Supply Current        | REF = 0 MHz                                              |     | 25.0  | μA   |
| $I_{DD}$           | Supply Current                   | Unloaded outputs at 66.67 MHz,<br>SEL inputs at $V_{DD}$ |     | 35.0  | mA   |

1. All parameters are specified with loaded outputs.

2. REF input has a threshold voltage of  $V_{PP}/2$ .

3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

**Table 7. Switching Characteristics for MPC962305-1 and MPC962309-1 Industrial Temperature Devices<sup>1</sup>**

| Parameter         | Name                                                      | Test Conditions                                                                    | Min      | Typ  | Max           | Unit       |
|-------------------|-----------------------------------------------------------|------------------------------------------------------------------------------------|----------|------|---------------|------------|
| t <sub>1</sub>    | Output Frequency                                          | 30-pF load<br>10-pF load                                                           | 10<br>10 |      | 100<br>133.33 | MHz<br>MHz |
|                   | Duty Cycle <sup>2</sup> = t <sub>2</sub> ÷ t <sub>1</sub> | Measured at 1.4 V, F <sub>OUT</sub> = 66.67 MHz                                    | 40.0     | 50.0 | 60.0          | %          |
| t <sub>3</sub>    | Rise Time <sup>2</sup>                                    | Measured between 0.8 V and 2.0 V                                                   |          |      | 2.50          | ns         |
| t <sub>4</sub>    | Fall Time <sup>2</sup>                                    | Measured between 0.8 V and 2.0 V                                                   |          |      | 2.50          | ns         |
| t <sub>5</sub>    | Output to Output Skew <sup>2</sup>                        | All outputs equally loaded                                                         |          |      | 250           | ps         |
| t <sub>6A</sub>   | Delay, REF Rising Edge to CLKOUT Rising Edge <sup>2</sup> | Measured at V <sub>DD</sub> /2                                                     |          | 0    | ±350          | ps         |
| t <sub>6B</sub>   | Delay, REF Rising Edge to CLKOUT Rising Edge <sup>2</sup> | Measured at V <sub>DD</sub> /2. Measured in PLL Bypass Mode, MPC962309 device only | 1        | 5    | 8.7           | ns         |
| t <sub>7</sub>    | Device to Device Skew <sup>2</sup>                        | Measured at V <sub>DD</sub> /2 on the CLKOUT pins of devices                       |          | 0    | 700           | ps         |
| t <sub>J</sub>    | Cycle to Cycle Jitter <sup>2</sup>                        | Measured at 66.67 MHz, loaded outputs                                              |          |      | 200           | ps         |
| t <sub>LOCK</sub> | PLL Lock Time <sup>2</sup>                                | Stable power supply, valid clock presented on REF pin                              |          |      | 1.0           | ms         |

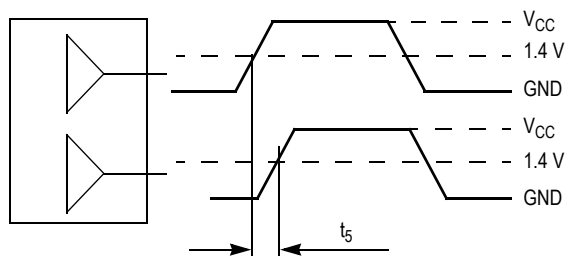
1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

**Table 8. Switching Characteristics for MPC962305-1H and MPC962309-1H Industrial Temperature Devices<sup>1</sup>**

| Parameter         | Name                                                      | Test Conditions                                                                    | Min      | Typ  | Max           | Unit       |
|-------------------|-----------------------------------------------------------|------------------------------------------------------------------------------------|----------|------|---------------|------------|
| t <sub>1</sub>    | Output Frequency                                          | 30-pF load<br>10-pF load                                                           | 10<br>10 |      | 100<br>133.33 | MHz<br>MHz |
|                   | Duty Cycle <sup>2</sup> = t <sub>2</sub> ÷ t <sub>1</sub> | Measured at 1.4 V, F <sub>OUT</sub> = 66.67 MHz                                    | 40.0     | 50.0 | 60.0          | %          |
|                   | Duty Cycle <sup>2</sup> = t <sub>2</sub> ÷ t <sub>1</sub> | Measured at 1.4 V, F <sub>OUT</sub> < 50 MHz                                       | 45.0     | 55.0 | 55.0          | %          |
| t <sub>3</sub>    | Rise Time <sup>2</sup>                                    | Measured between 0.8 V and 2.0 V                                                   |          |      | 1.50          | ns         |
| t <sub>4</sub>    | Fall Time <sup>2</sup>                                    | Measured between 0.8 V and 2.0 V                                                   |          |      | 1.50          | ns         |
| t <sub>5</sub>    | Output to Output Skew <sup>2</sup>                        | All outputs equally loaded                                                         |          |      | 250           | ps         |
| t <sub>6A</sub>   | Delay, REF Rising Edge to CLKOUT Rising Edge <sup>2</sup> | Measured at V <sub>DD</sub> /2                                                     |          | 0    | ±350          | ps         |
| t <sub>6B</sub>   | Delay, REF Rising Edge to CLKOUT Rising Edge <sup>2</sup> | Measured at V <sub>DD</sub> /2. Measured in PLL Bypass Mode, MPC962309 device only | 1        | 5    | 8.7           | ns         |
| t <sub>7</sub>    | Device to Device Skew <sup>2</sup>                        | Measured at V <sub>DD</sub> /2 on the CLKOUT pins of devices                       |          | 0    | 700           | ps         |
| t <sub>8</sub>    | Output Slew Rate <sup>2</sup>                             | Measured between 0.8 V and 2.0 V using Test Circuit #2                             | 1        |      |               | V/ns       |
| t <sub>J</sub>    | Cycle to Cycle Jitter <sup>2</sup>                        | Measured at 66.67 MHz, loaded outputs                                              |          |      | 200           | ps         |
| t <sub>LOCK</sub> | PLL Lock Time <sup>2</sup>                                | Stable power supply, valid clock presented on REF pin                              |          |      | 1.0           | ms         |

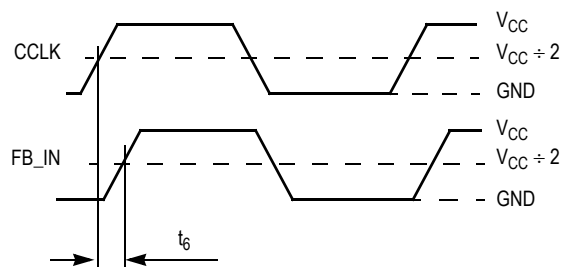
1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

### APPLICATIONS INFORMATION

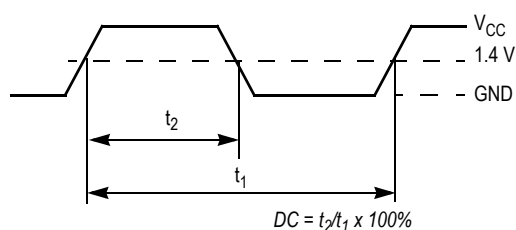


The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

**Figure 1. Output-to-Output Skew  $t_{SK(O)}$**

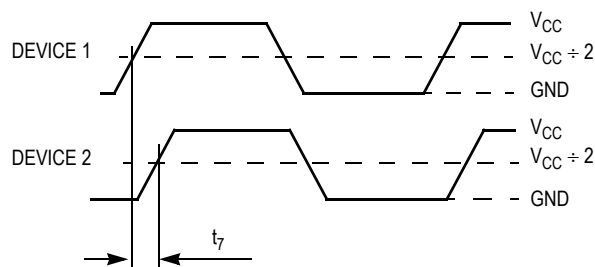


**Figure 2. Static Phase Offset Test Reference**

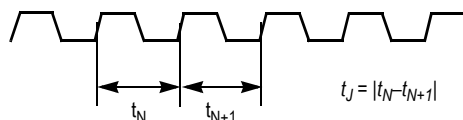


The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

**Figure 3. Output Duty Cycle (DC)**

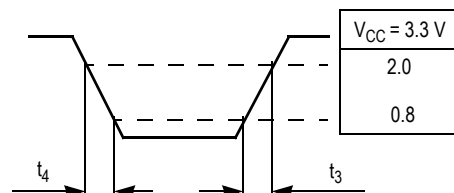


**Figure 4. Device-to-Device Skew**

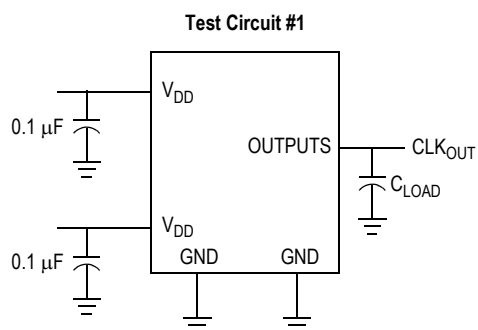


The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

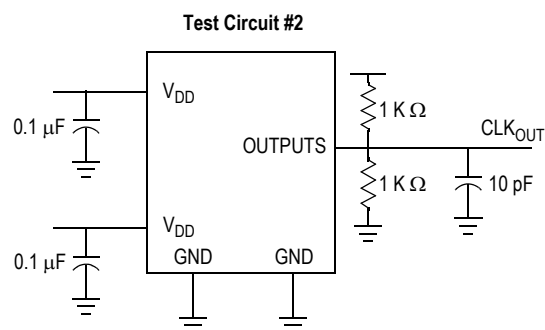
**Figure 5. Cycle-to-Cycle Jitter**



**Figure 6. Output Transition Time Test Reference**



Test Circuit for all parameters except  $t_b$



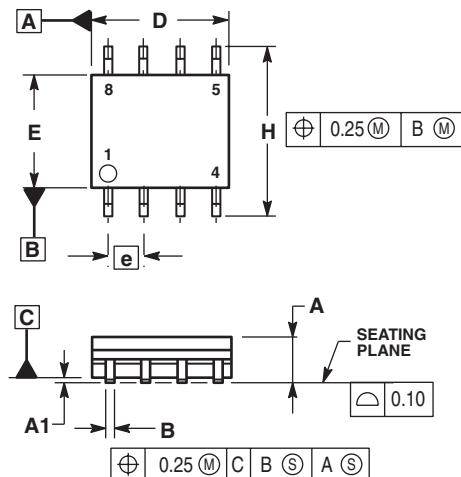
Test Circuit for  $t_b$ , Output slew rate on -1H, -5 device

**Table 9. Ordering Information**

| Ordering Code    | Package Type                      |
|------------------|-----------------------------------|
| MPC962305D-1     | 8-pin 150-mil SOIC                |
| MPC962305D-1R2   | 8-pin 150-mil SOIC-Tape and Reel  |
| MPC962305D-1H    | 8-pin 150-mil SOIC                |
| MPC962305D-1HR2  | 8-pin 150-mil SOIC-Tape and Reel  |
| MPC962305DT-1H   | 8-pin 150-mil TSSOP               |
| MPC962305DT-1HR2 | 8-pin 150-mil TSSOP-Tape and Reel |
| MPC962309D-1     | 16-pin 150-mil SOIC               |
| MPC962309D-1R2   | 16-pin 150-mil SOIC-Tape and Reel |
| MPC962309D-1H    | 16-pin 150-mil SOIC               |
| MPC962309D-1HR2  | 16-pin 150-mil SOIC-Tape and Reel |
| MPC962309DT-1H   | 16-pin 4.4-mm TSSOP               |
| MPC962309DT-1HR2 | 16-pin 4.4-mm TSSOP-Tape and Reel |

### PACKAGE DIMENSIONS

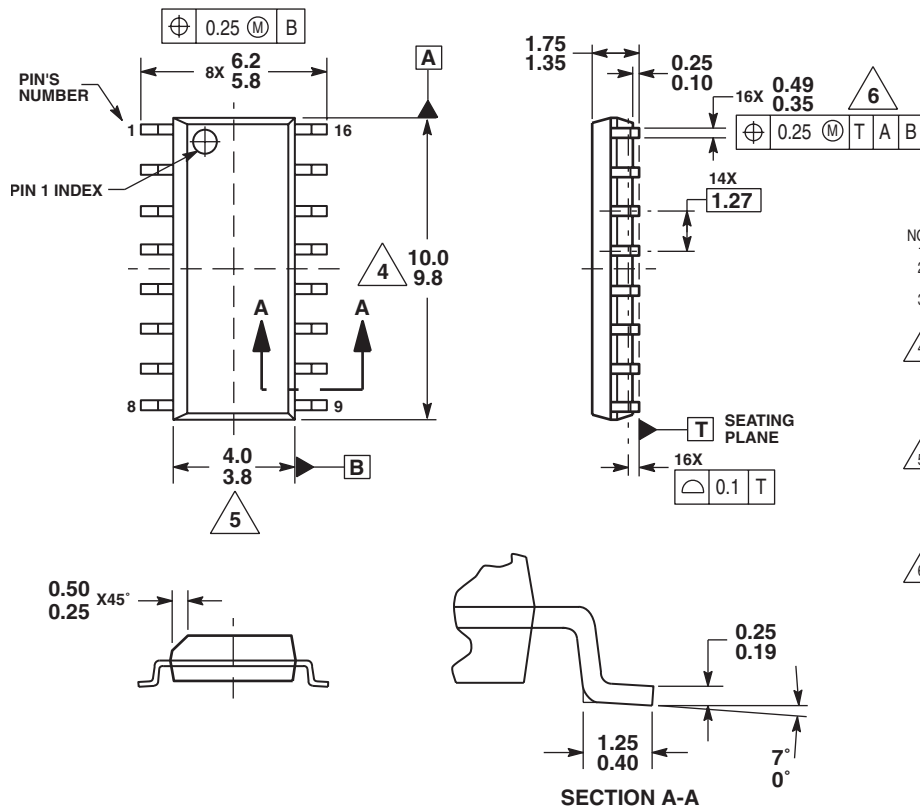
#### D SUFFIX 8-LEAD SOIC PACKAGE CASE 751-06 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. DIMENSIONS ARE IN MILLIMETER.
  3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MIN      | MAX  |
|-----|----------|------|
| A   | 1.35     | 1.75 |
| A1  | 0.10     | 0.25 |
| B   | 0.35     | 0.49 |
| C   | 0.19     | 0.25 |
| D   | 4.80     | 5.00 |
| E   | 3.80     | 4.00 |
| e   | 1.27 BSC |      |
| H   | 5.80     | 6.20 |
| h   | 0.25     | 0.50 |
| L   | 0.40     | 1.25 |
| q   | 0°       | 7°   |

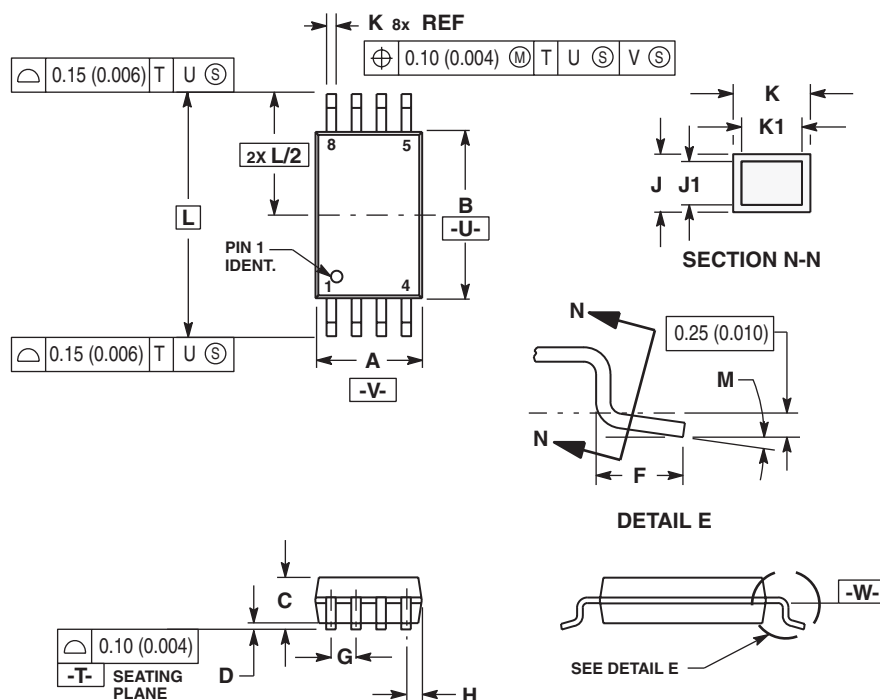
#### D SUFFIX 16-LEAD SOIC PACKAGE CASE 751B-05 ISSUE K



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62MM.

### PACKAGE DIMENSIONS

DT SUFFIX  
8-LEAD TSSOP PACKAGE  
CASE 948J-01  
ISSUE O



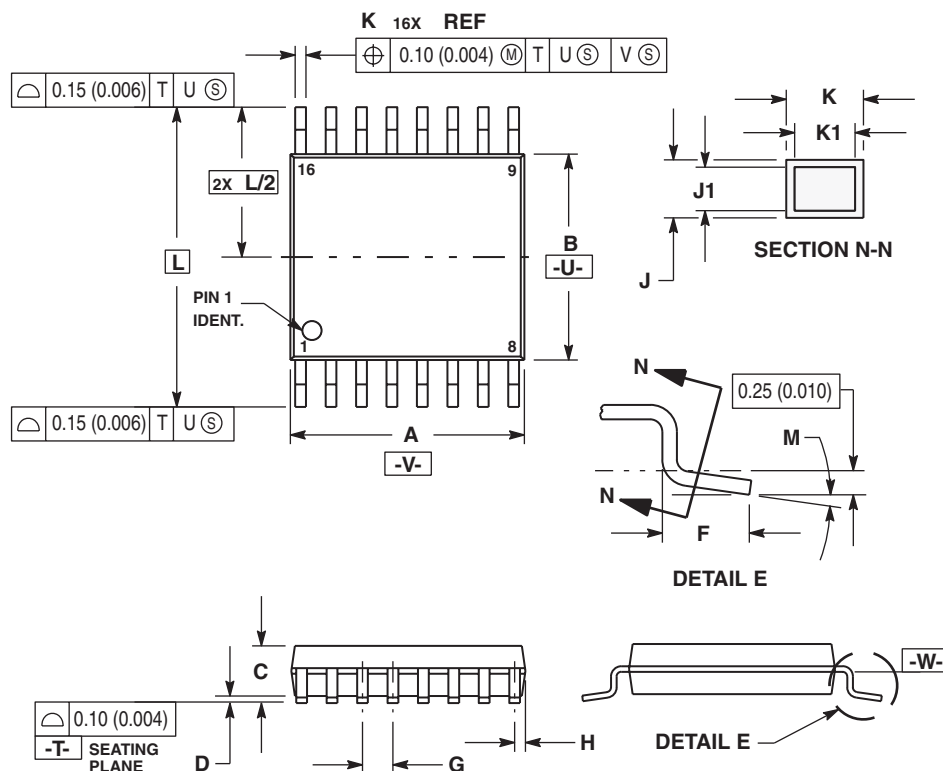
#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0"          | 8"   | 0"        | 8"    |

### PACKAGE DIMENSIONS

DT SUFFIX  
16-LEAD TSSOP PACKAGE  
CASE 948F-01  
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0"          | 8"   | 0"        | 8"    |

**NOTES**

**NOTES**

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

MOTOROLA and the Stylized M Logo are registered in the US Patent and Trademark Office. All other product or service names are the property of their respective owners.

© Motorola, Inc. 2004

#### HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:  
Motorola Literature Distribution  
P.O. Box 5405, Denver, Colorado 80217  
1-800-521-6274 or 480-768-2130

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center  
3-20-1 Minami-Azabu, Minato-ku, Tokyo 106-8573, Japan  
81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre  
2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong  
852-26668334

HOME PAGE: <http://motorola.com/semiconductors>



**MOTOROLA**

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**

**MPC962305**